SuperFAP-G Series of Power MOSFETs

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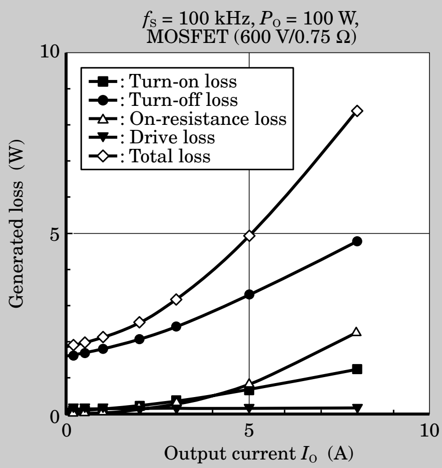
1. Introduction

In recent years, shipments of information and communication equipment, mainly network related equipment such as personal computers and servers, have been rapidly increasing as IT (information technology) progresses. Accordingly, reduction of power dissipation in the equipment is strongly required in order to achieve resource-saving, energy-saving and downsizing. The SMPS (switched mode power supply) used in this equipment is required to have high efficiency and low loss. Moreover, for OA (office automation) equipment that has long standby times, such as facsimile and copy machines, a reduction of the power dissipation during standby is also required, and the trend toward higher efficiency and lower loss is growing, supported with regulations such as the revised energy-saving law.

Figure 1 shows the simulated results of power MOSFET (metal oxide semiconductor field effect transistor) loss in a forward converter, a typical SMPS. The turn-off loss constitutes about 50 % of the total loss under the steady load condition (output current of 8 A). Moreover, the on-state resistance ($R_{DS(on)}$) loss constitutes about 32 % of the total loss. Thus, 80 % or more of the total loss is comprised of the turn-off loss and the on-state resistance loss. This fact demonstrates the necessity of improving both types of loss in order to achieve high efficiency and low loss of an SMPS. On the other hand, the turn-off loss constitutes about 90 % of the total loss at a light load condition equal to the standby power dissipation. To accommodate downsizing of the information and communication equipment, SMPS is adopting high switching frequency, and the trend in recent years has been toward even higher frequencies. In the future, reduction of the switching loss, typified by the turn-off loss, is expected to become even more important.

This paper will present an overview of the features of the low loss and ultra-high speed power MOSFET SuperFAP-G series, developed to satisfy the abovementioned market needs, and its effectiveness in applications.

Fig.1 Simulation results of forward converter loss



2. Features

The turn-off loss of a power MOSFET is determined by the charging time constant of the reverse transfer capacitance (C_{rss}) between the drain and gate. Accordingly, the amount of electric charge (Q_{gd}) between the drain and gate must be reduced in order to decrease the turn-off loss. There is a trade-off relationship between Q_{gd} and $R_{DS(on)}$ and improvement of the trade-off is essential to achieve the desired power MOSFET specifications of reduced on-state resistance and turn-off loss. Accordingly, the definition of the figure-of-merit (FOM) of a power MOSFET, previously represented as $R_{on} \cdot A$, has been reestablished as the product of $R_{DS(on)}$ and Q_{gd}. This means that a smaller value of $R_{on} \cdot Q_{gd}$ indicates a higher performance power MOSFET.

In Table 1, characteristics of a SuperFAP-G device are compared with those of a conventional product having the same on-state resistance. The representative model, newly developed and having a drain-source breakdown voltage of 150 V, has a FOM of 0.675 Ω · nC, indicating that performance has been improved by about 2.5 times compared to the conventional product. Design techniques for realizing such improvement in the FOM will be described below.

3. Design Technologies

In the SuperFAP-G series, a new technique referred to as quasi-plain-junction (QPJ) was developed to improve the on-state resistance loss. Figure 2 shows the structure of the QPJ.

Most of the on-state resistance in a power MOS FET with medium or high drain-source voltage is limited by the resistivity of n− type silicon in the epitaxial layers. Therefore, reducing n− type silicon resistivity achieves low on-state resistance, but this approach leads to the problem of decreased drain-source breakdown voltage. Theoretically, the on-state resistance per unit area ($R_{on} \cdot A$) is proportional to the 2.5th power of the breakdown voltage, so low resistivity n− type silicon, near the theoretical limit, must be used to decrease the on-state resistance of power MOSFETs as much as possible. The cell structure of a conventional power MOSFET contains much three-dimensional unevenness and therefore the electric field is highly concentrated and only about 80 % of the theoretical limit of the breakdown voltage had been achieved. To supplement the voltage, it was necessary to increase n− type silicon resistivity to more than 175 % of the theoretical limit, but as a consequence, the on-state resistance per unit area could not be decreased. In the QPJ structure of the SuperFAP-G series, a cell with a junction having a nearly planer surface has been realized by arranging low-concentration shallow p− wells densely, in place of the conventional high-concentration deep p+ wells. The QPJ structure has achieved a breakdown voltage of 97 % relative to the silicon theoretical limit, and as a result, has reduced the n− type silicon resistivity to 108 % of the theoretical limit and achieved low on-state resistance within 10 % of the silicon theoretical limit value shown in Fig. 3. On the other hand, in order to reduce

Table 1 Comparison of SuperFAP-G characteristics

Series / Item	SuperFAP-G 2SK3474-01	Conventional product 2SK2226-01
V_{DS}	150 V	150 V
I_D	33 A	20 A
P_D	150 W	80 W
$V_{GS(th)}$	3 to 5 V	1 to 2.5 V
$R_{DS(on)}$(typ.)	54 mΩ	55 mΩ
Q_g	34 nC	100 nC
Q_{gd}	12.5 nC	30 nC
FOM $R_{on} \cdot Q_{gd}$	0.675 Ω · nC	1.65 Ω · nC

Fig.3 Relation between V_b and $R_{on} \cdot A$

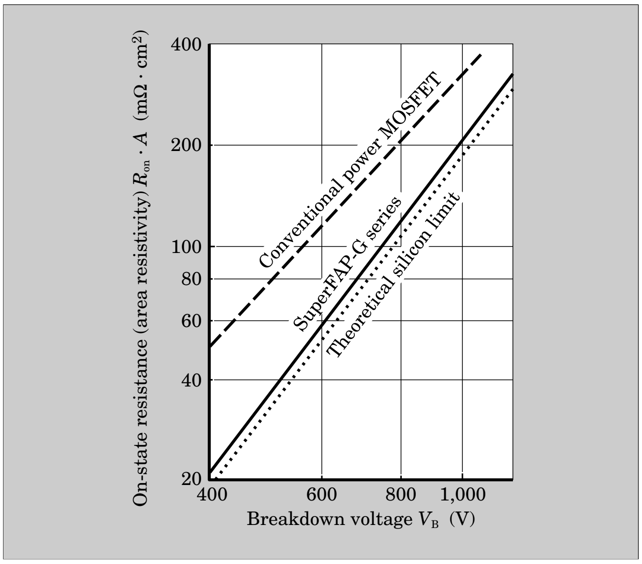


Fig.2 SuperFAP-G chip structure (QPJ structure)

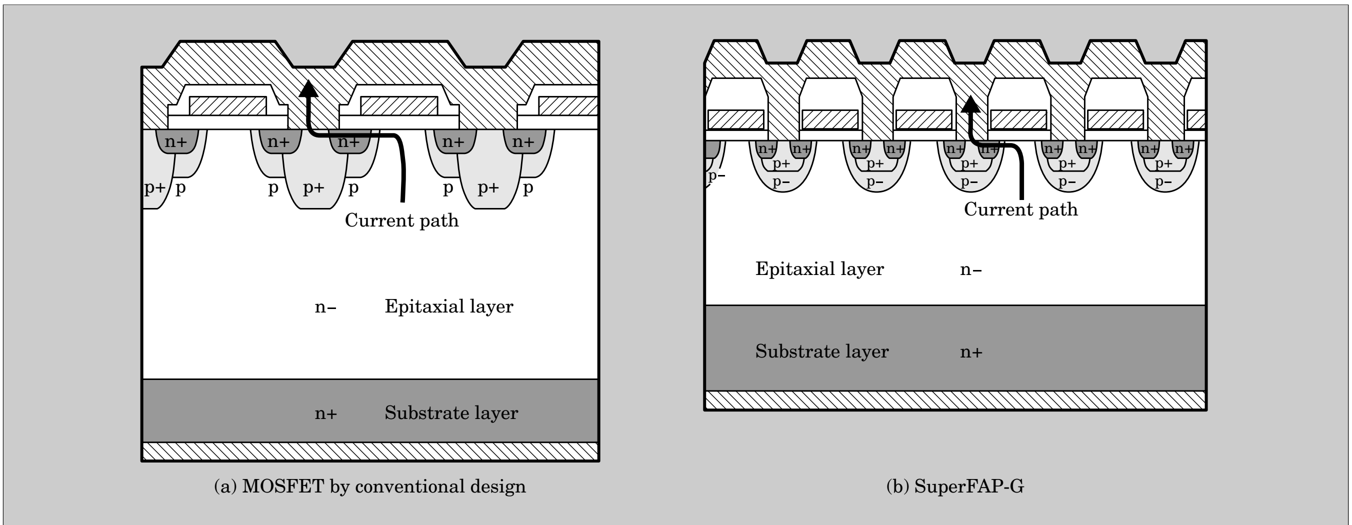


Table 2 SuperFAP-G series

Drain-source voltage BV_{DSS}	Drain current I_D	On-state resistance $R_{DS\,(on)}$ (max.)	Gate charge		Package				
			Q_G	Q_{gd}	TO-220	TO-220F	D^2-pack	TFP	TO-247
100 V	29 A	62 mΩ	22 nC	6 nC	2SK3598	2SK3599	2SK3600	2SK3601	–
	41 A	44 mΩ	32 nC	9 nC	2SK3644	2SK3645	2SK3646	2SK3647	–
	73 A	25 mΩ	52 nC	18 nC	2SK3586	2SK3587	2SK3588	2SK3589	–
150 V	23 A	105 mΩ	21 nC	6 nC	2SK3602	2SK3603	2SK3604	2SK3605	–
	33 A	70 mΩ	34 nC	12.5 nC	2SK3648	2SK3649	2SK3650	2SK3474	–
	57 A	41 mΩ	52 nC	18 nC	2SK3590	2SK3591	2SK3592	2SK3593	–
200 V	18 A	170 mΩ	21 nC	5 nC	2SK3606	2SK3607	2SK3608	2SK3609	–
	45 A	66 mΩ	51 nC	16 nC	2SK3594	2SK3595	2SK3596	2SK3597	–
250 V	14 A	260 mΩ	21 nC	5 nC	2SK3610	2SK3611	2SK3612	2SK3613	–
	37 A	100 mΩ	44 nC	16 nC	2SK3554	2SK3555	2SK3556	2SK3535	–
700 V	10 A	1.18 Ω	35 nC	10 nC	–	2SK3673	–	–	–
	12 A	0.93 Ω	31 nC	9 nC	–	2SK3577	–	–	–
800 V	7 A	1.9 Ω	25 nC	7 nC	2SK3529	2SK3530	–	–	–
900 V	6 A	2.5 Ω	25 nC	7 nC	2SK3531	2SK3532	2SK3676	–	–
	7 A	2.0 Ω	28 nC	8 nC	2SK3533	2SK3534	2SK3674	–	2SK3675
	9 A	1.58 Ω	32 nC	7 nC	2SK3678	2SK3679	–	–	–
	10 A	1.4 Ω	37 nC	10 nC	–	–	–	–	2SK3549

Fig.4 External view of SuperFAP-G

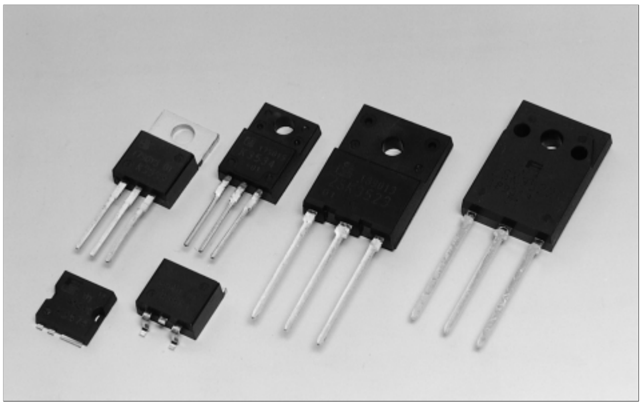
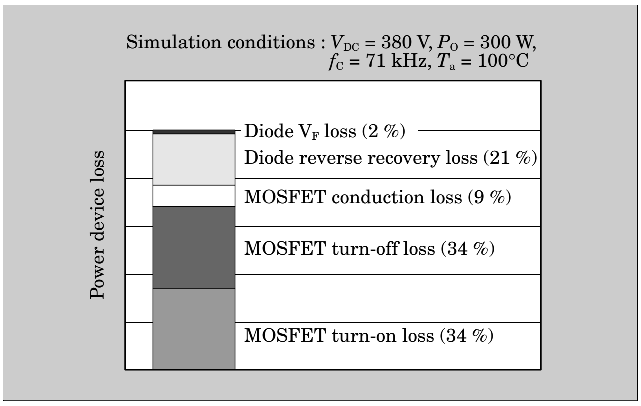


Fig.5 Simulation results of loss in continuous current mode PFC circuit



Q_{gd} that determines the turn-off loss, it is necessary to narrow the n− type silicon width (current path) and make it shorter. However, there is a trade-off relationship between Q_{gd} and $R_{DS(on)}$, and a narrower current path creates the problem of increased on-state resistance. In the QPJ structure, in addition to shortening the current path with shallow p− wells, high-concentration n type doping narrows the n− type silicon current path to its limit without increasing the on-state resistance. As a result, Qgd has been reduced by about 60 % compared to conventional products with the same on-state resistance.

3.1 SuperFAP-G series

In the SuperFAP-G series, about 40 types of products with drain-source voltage range from 450 to 600 V have been developed and are already being commercially produced. The following products have been added to the product series at this time: 100 to 250 V, medium drain-source voltage class power MOSFETs for use in DC-DC converters supporting a 12 to 72 V DC input, and 700 to 900 V drain-source voltage class power MOSFETs for use in SMPS with a 200 V AC input. Typical ratings of the SuperFAP-G series newly added to the product line are shown in Table 2. External views of the SuperFAP-G series are shown in Fig. 4.

4. Application and Merit of SuperFAP-G Series

As example applications, the results of applying the newly developed SuperFAP-G series in typical circuits, such as PFC (power factor correction) and DC-

DC converter circuits, will be introduced below.

4.1 Application to PFC circuit

A capacitor-input type SMPS is usually equipped with a PFC circuit using a booster type converter to regulate input higher harmonic current. The addition of a PFC circuit means that the power-conversion circuit will be in two blocks, so loss reduction and efficiency improvement in the PFC circuit are strongly required. Figure 5 shows analyzed results of the loss generated from switching devices in a continuous current mode PFC circuit. The power MOSFET loss constitutes about 70 % of the generated loss, and 90 % of which is attributed to both of the turn-on and turn-off switching loss.

As shown in Fig. 6, the turn-on loss of a power MOSFET is strongly affected by reverse recovery characteristics of the output diode in a continuous current mode PFC circuit. Thus, in order to reduce the turn-on loss, it is important to decrease the reverse recovery current of the diode (I_{rp}). We have developed and commercialized the super high-speed diode SuperLLD series, having improved reverse recovery characteristics and designed for optimum use of continuous current mode PFCs. Use of the SuperLLD series reduces the turn-on loss of a power MOSFET by about 40 % compared with conventional diodes.

On the other hand, turn-off loss, as shown by the waveforms in Fig. 7, is determined by the switching characteristics of the power MOSFET itself. Application of the SuperFAP-G series allows the turn-off time to speed up by about 60 % and the generated loss to decrease by about 80 % compared with conventional power MOSFETs having the same rating.

Use of the SuperFAP-G series in conjunction with the SuperLLD series in commercial SMPS equipped with continuous current mode PFC circuits resulted in an approximate 1 % improvement in efficiency and a 6 % decrease in the heat sink temperature-rise, as shown in Fig. 8 and Fig. 9.

Examples of recommended combinations of the SuperFAP-G and SuperLLD series in continuous current mode PFC circuits are listed in Table 3.

4.2 Application to DC-DC converter

Brick type DC-DC converters are used in the on-board power supplies of information and communication equipment. At present, the trends toward downsizing and increased power density are proceeding concurrently, and most leading DC-DC converters are moving away from conventional full-brick types and toward half-brick (1/2) or smaller types that have the

Fig.6 Continuous current mode PFC circuit (turn-on waveform)

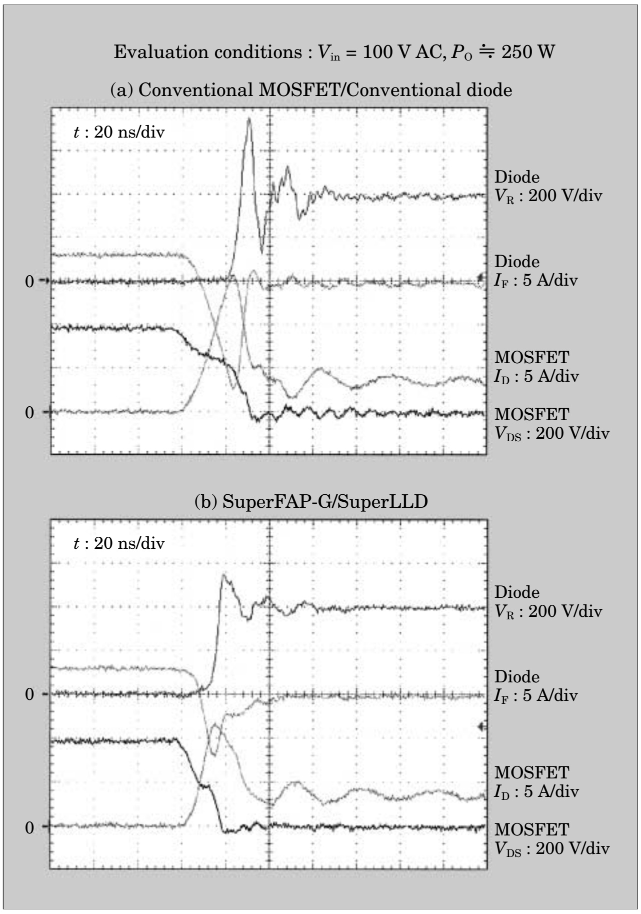
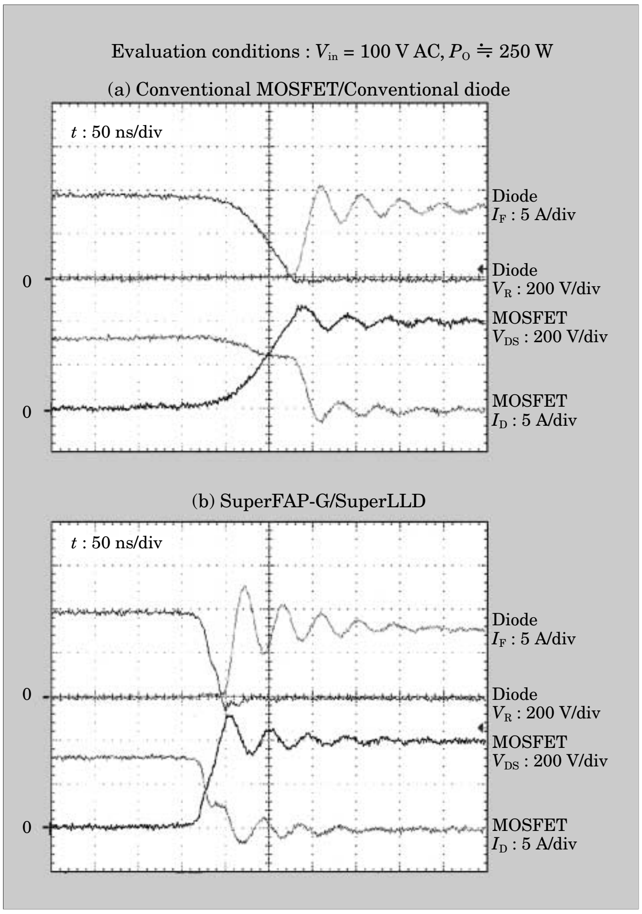


Fig.7 Continuous current mode PFC circuit (turn-off waveform)



same power capacity with smaller external dimensions. To achieve downsizing and power density improvement, it is necessary to downsize the passive components (such as capacitor, inductor, transformer) and reduce the switching device loss by using a higher switching frequency.

To reduce the switching device loss, the switching loss and drive loss must be decreased, since the switching is operated at a high frequency of more than 300 kHz.

Fig.8 Continuous current mode PFC (measured results of temperature-rise)

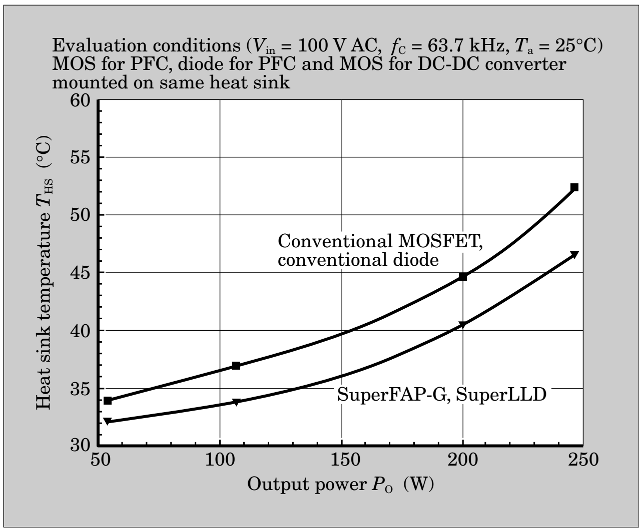


Fig.9 Continuous current mode PFC (measured results of conversion efficiency)

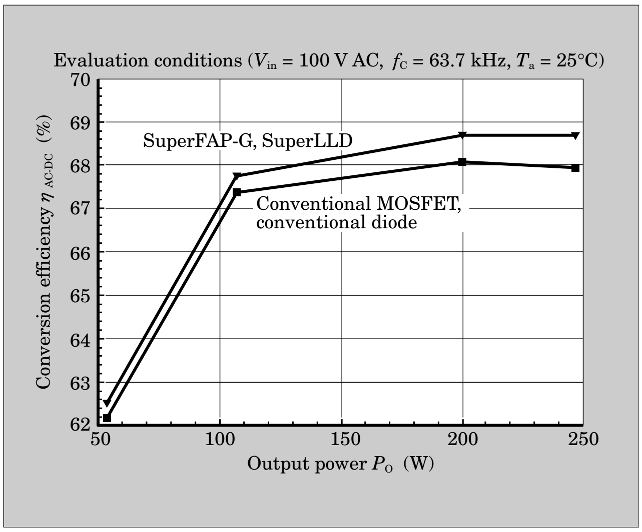


Fig. 10 Evaluation results of installation in DC-DC converter (low output)

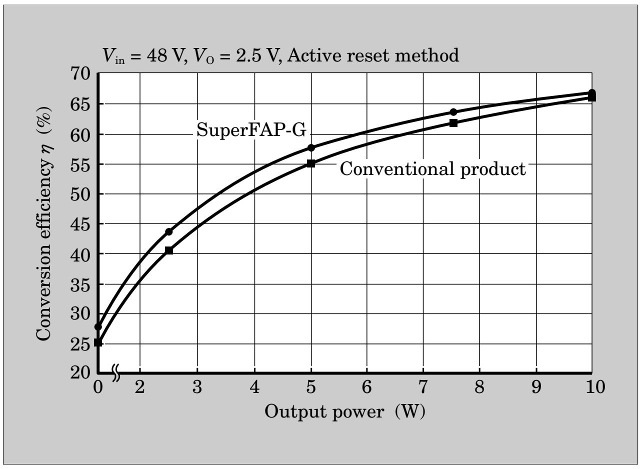


Fig.11 Evaluation result of installation in DC-DC converter (high output)

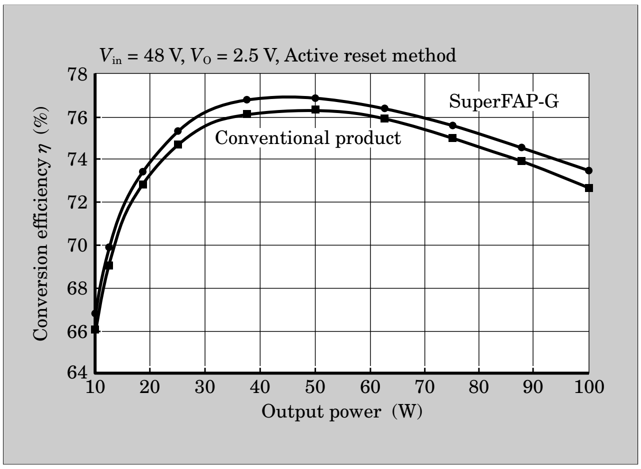


Table 3 SuperFAP-G/SuperLLD for continuous current mode PFC

Power supply capacity P_O	Model	Electrical characteristics				Package
≤150W	2SK3504-01	V_{DS} = 500 V	I_D = 14 A	$R_{DS\,(on)}$ = 0.46 Ω (max.)	Q_{gd} = 10.5 nC (typ.)	TO-220
	YA961S6	V_R = 600 V	I_P = 8 A	V_F = 2.0 V (typ.)	t_{rr} = 23 ns (max.)	TO-220
≤250W	2SK3522-01	V_{DS} = 500 V	I_D = 21 A	$R_{DS\,(on)}$ = 0.26 Ω (max.)	Q_{gd} = 20 nC (typ.)	TO-247
	YA962S6	V_R = 600 V	I_P = 10 A	V_F = 1.6 V (typ.)	t_{rr} = 25 ns (max.)	TO-220
≤350W	2SK3680-01	V_{DS} = 500 V	I_D = 43 A	$R_{DS\,(on)}$ = 0.11 Ω (max.)	Q_{gd} = 50 nC (typ.)	TO-247
	YA963S6	V_R = 600 V	I_P = 15 A	V_F = 1.7 V (typ.)	t_{rr} = 30 ns (max.)	TO-220

Figures 10 and 11 show evaluation results of the recently developed 150 V / 70 mΩ SuperFAP-G series, which was installed in a typical, commercially available quarter-brick type DC-DC converter (48 V input, 2.5 V output, 150 W).

Compared to a conventional power MOSFET with the same ratings, an approximate 60 % reduction in gate charge and a maximum 4 % improvement in conversion efficiency have been achieved. To meet the needs for downsizing, small TFP-packaged products for surface mounting are also included in the product line.

5. Conclusion

This paper has presented an overview of the design and application effect of Fuji Electric's SuperFAP-G series of low-loss and ultra high-speed switching power MOSFETs. Application of the SuperFAP-G series to SMPS or DC-DC converters will increase conversion efficiency and reduce both power dissipation and temperature-rise. We are certain that this series will contribute to energy savings and downsizing of equipment.

In the future, Fuji Electric will work to expand this product line to meet a wider range of power supply specifications.

Reference

(1) Kobayashi, T. et al. High-Voltage Power MOSFETs Reached Almost to the Silicon Limit. Proceedings of the 13th ISPSD. 2001, p.435-438.